

100V N-Channel Enhancement Mode MOSFET

General Description

20N10D use advanced SGT MOSFET technology to provide low $R_{DS(ON)}$, low gate charge, fast switching and excellent avalanche characteristics.

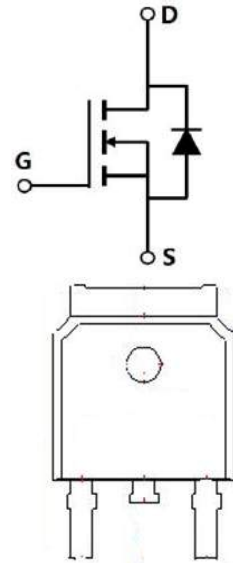
This device is specially designed to get better ruggedness and suitable to use in

Features

- Low $R_{DS(on)}$ & FOM
- Extremely low switching loss
- Excellent stability and uniformity or Invertors

Applications

- Consumer electronic power supply
- Motor control
- Synchronous-rectification
- Isolated DC
- Synchronous-rectification applications



Absolute Maximum Ratings at $T_j=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain source voltage	V_{DS}	100	V
Gate source voltage	V_{GS}	± 20	V
Continuous drain current ¹⁾ , $T_C=25^\circ\text{C}$	I_D	20	A
Pulsed drain current ²⁾ , $T_C=25^\circ\text{C}$	$I_{D, pulse}$	45	A
Power dissipation ³⁾ , $T_C=25^\circ\text{C}$	P_D	17	W
Single pulsed avalanche energy ⁴⁾	E_{AS}	4.2	mJ
Operation and storage temperature	T_{stg}, T_j	-55 to 150	$^\circ\text{C}$
Thermal resistance, junction-case	$R_{\theta JC}$	7.4	$^\circ\text{C/W}$
Thermal resistance, junction-ambient ⁵⁾	$R_{\theta JA}$	62	$^\circ\text{C/W}$

100V N-Channel Enhancement Mode MOSFET

Electrical Characteristics at $T_j=25\text{ }^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test condition
Drain-source breakdown voltage	BV_{DSS}	100			V	$V_{GS}=0\text{ V}$, $I_D=250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	1.0	1.7	3.0	V	$V_{DS}=V_{GS}$, $I_D=250\text{ }\mu\text{A}$
Drain-source on-state resistance	$R_{DS(on)}$		55	75	$\text{m}\Omega$	$V_{GS}=10\text{ V}$, $I_D=5\text{ A}$
Drain-source on-state resistance	$R_{DS(on)}$		112	300	$\text{m}\Omega$	$V_{GS}=4.5\text{ V}$, $I_D=3\text{ A}$
Gate-source leakage current	I_{GSS}			100	nA	$V_{GS}=20\text{ V}$
				-100		$V_{GS}=-20\text{ V}$
Drain-source leakage current	I_{DSS}			200	nA	$V_{DS}=100\text{ V}$, $V_{GS}=0\text{ V}$
Input capacitance	C_{iss}		429.4		pF	$V_{GS}=0\text{ V}$,
Output capacitance	C_{oss}		58.3		pF	$V_{DS}=50\text{ V}$, $f=1$
Reverse transfer capacitance	C_{rss}		2.9		pF	MHz
Turn-on delay time	$t_{d(on)}$		15.6		ns	$V_{GS}=10\text{ V}$,
Rise time	t_r		4.2		ns	$V_{DS}=50\text{ V}$,
Turn-off delay time	$t_{d(off)}$		26.8		ns	$R_G=2\text{ }\Omega$,
Fall time	t_f		3.6		ns	$I_D=5\text{ A}$
Total gate charge	Q_g		7.6		nC	$I_D=5\text{ A}$, $V_{DS}=50\text{ V}$, $V_{GS}=10\text{ V}$
Gate-source charge	Q_{gs}		1.4		nC	
Gate-drain charge	Q_{gd}		2.4		nC	
Gate plateau voltage	$V_{plateau}$		4.5		V	
Diode forward current	I_S			15	A	$V_{GS}<V_{th}$
Pulsed source current	I_{SP}			45		
Diode forward voltage	V_{SD}			1.3	V	$I_S=7\text{ A}$, $V_{GS}=0\text{ V}$
Reverse recovery time	t_{rr}		36.1		ns	$I_S=5\text{ A}$, $di/dt=100$ A/ μs
Reverse recovery charge	Q_{rr}		50.4		nC	
Peak reverse recovery current	I_{rrm}		2.6		A	

■ Note

- 1) Calculated continuous current based on maximum allowable junction temperature.
- 2) Repetitive rating; pulse width limited by max. junction temperature.
- 3) P_d is based on max. junction temperature, using junction-case thermal resistance.
- 4) $V_{DD}=50\text{ V}$, $R_G=50\text{ }\Omega$, $L=0.3\text{ mH}$, starting $T_j=25\text{ }^\circ\text{C}$.
- 5) The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_a=25\text{ }^\circ\text{C}$.

Electrical Characteristics Diagrams

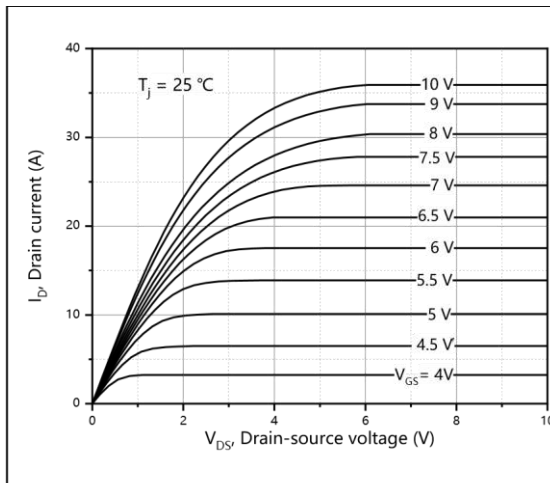


Figure 1, Typ. output characteristics

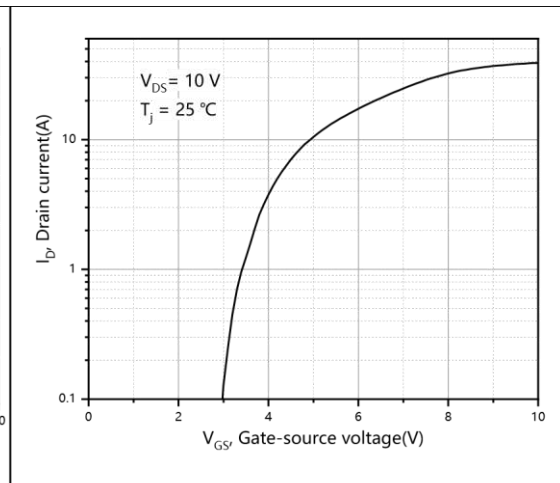


Figure 2, Typ. transfer characteristics

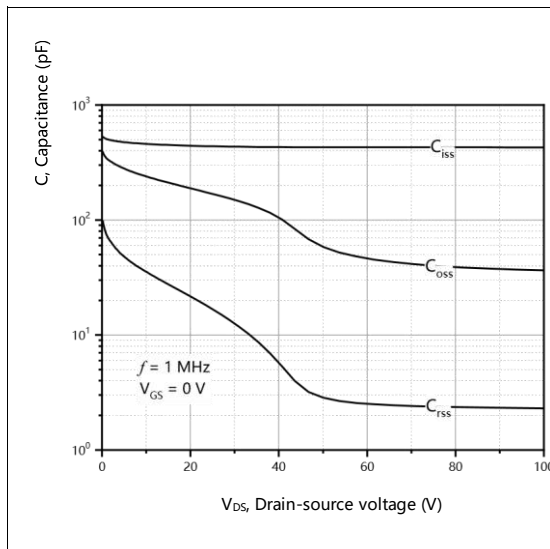


Figure 3, Typ. capacitances

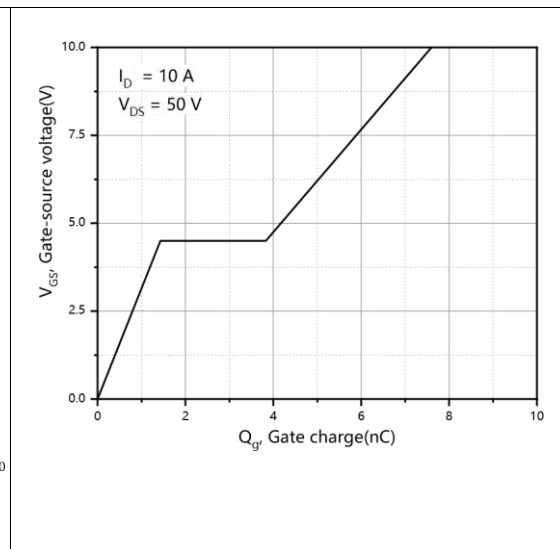


Figure 4, Typ. gate charge

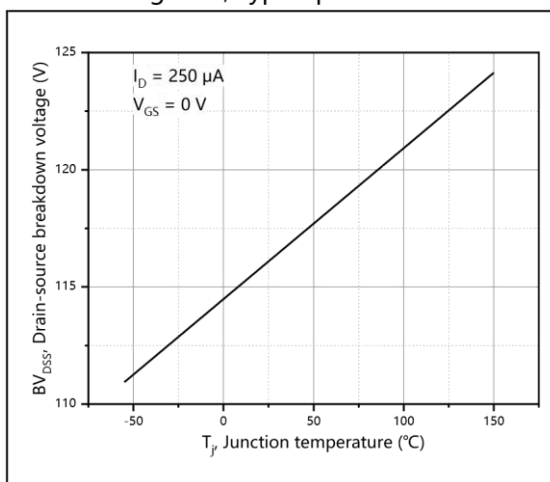


Figure 5, Drain-source breakdown voltage

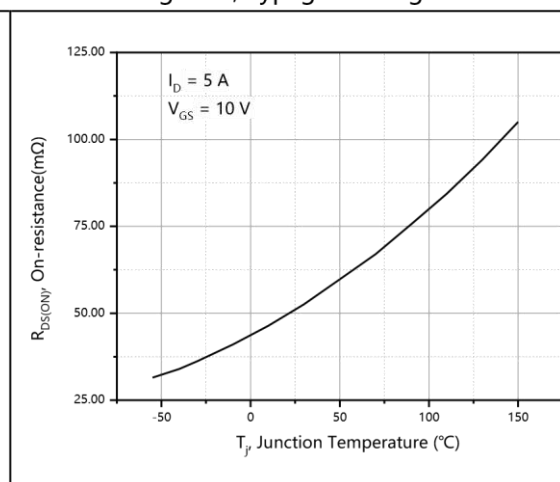


Figure 6, Drain-source on-state resistance

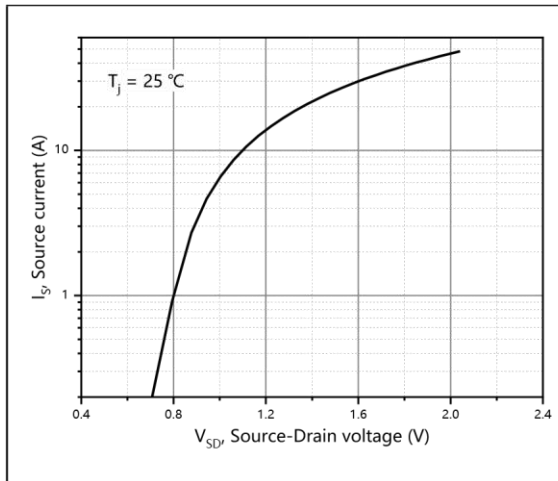


Figure 7, Forward characteristic of body diode

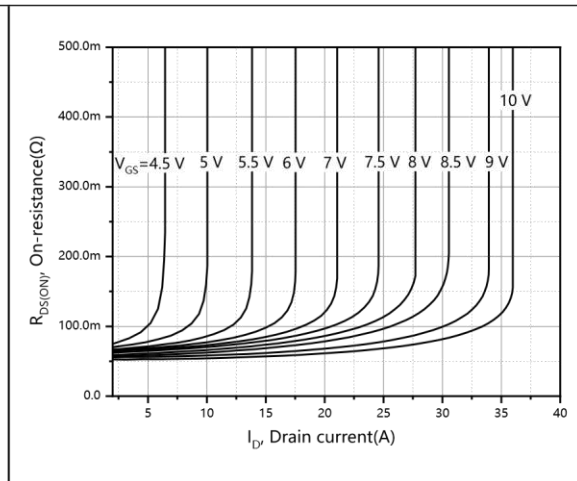


Figure 8, Drain-source on-state resistance

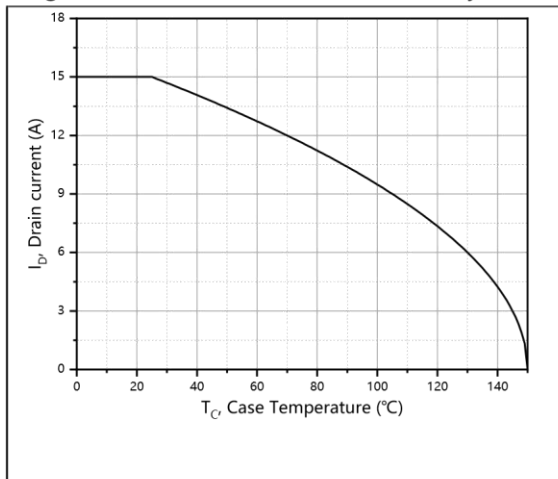


Figure 9, Drain current

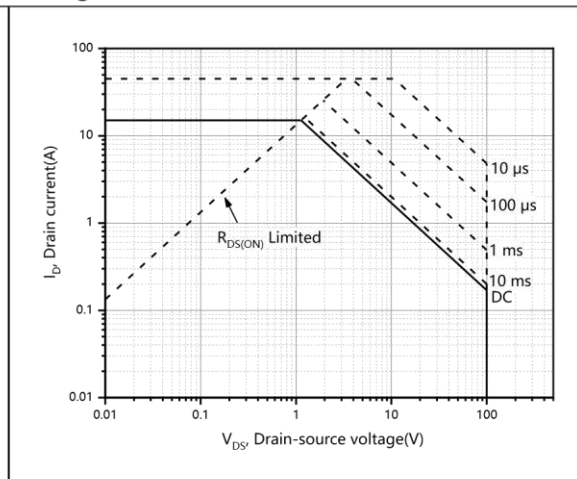


Figure 10, Safe operation area $T_C=25\text{ }^{\circ}\text{C}$

Test circuits and waveforms

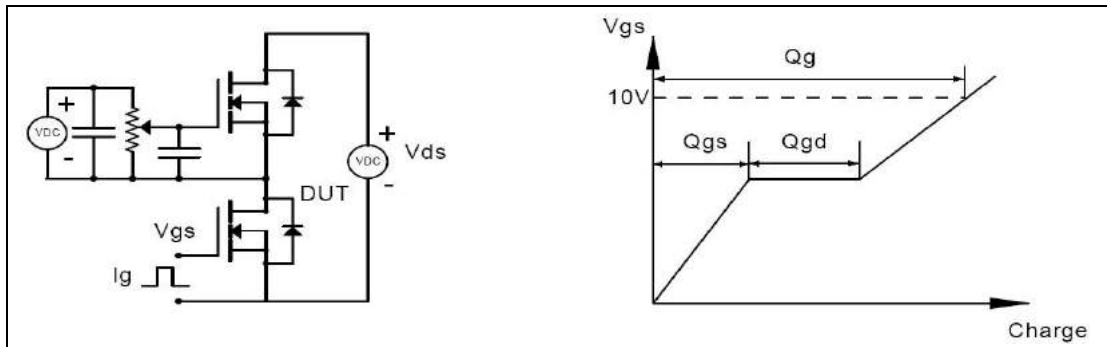


Figure 1, Gate charge test circuit & waveform

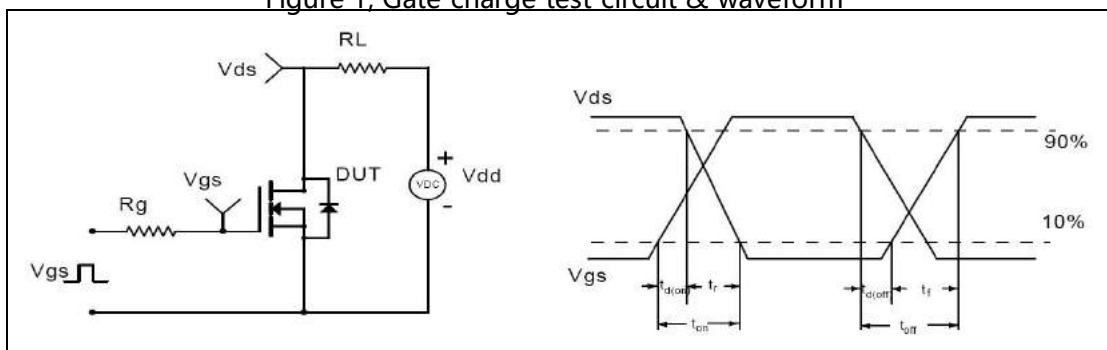


Figure 2, Switching time test circuit & waveforms

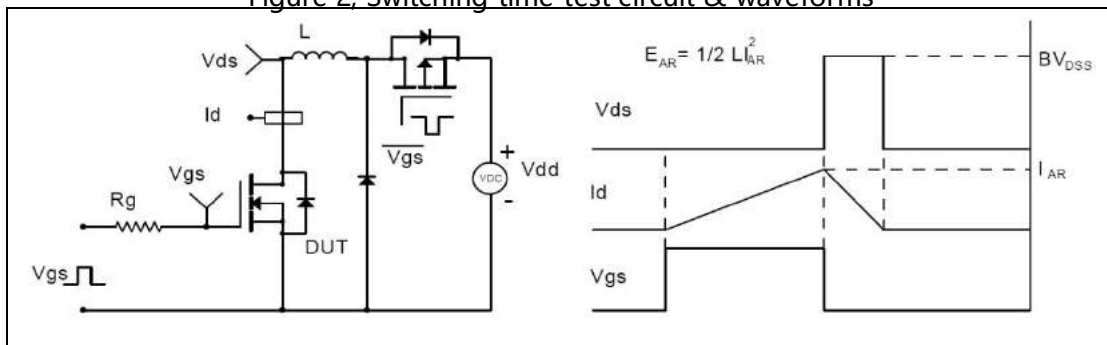


Figure 3, Unclamped inductive switching (UIS) test circuit & waveforms

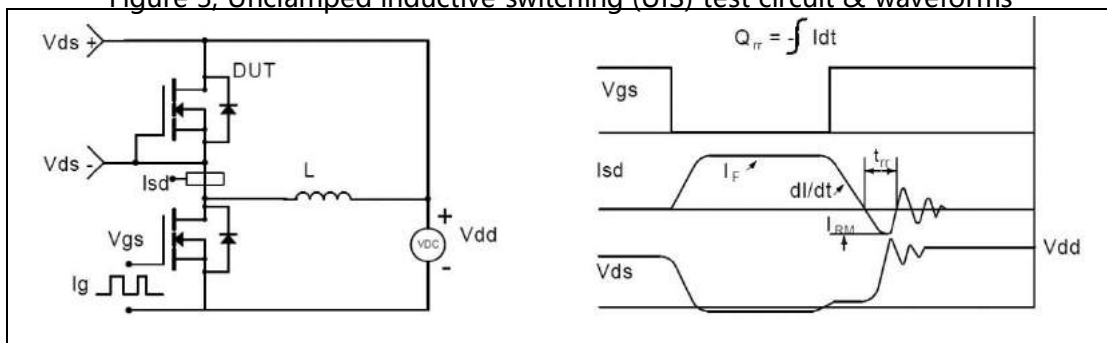
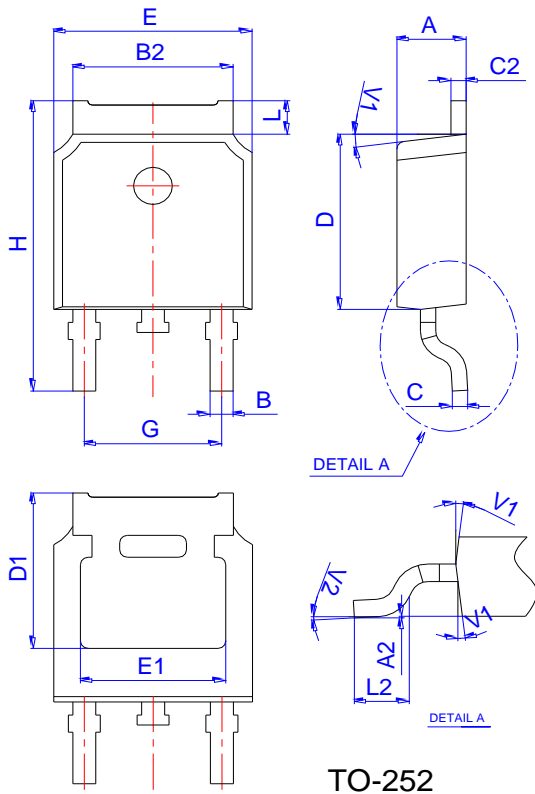


Figure 4, Diode reverse recovery test circuit & waveforms

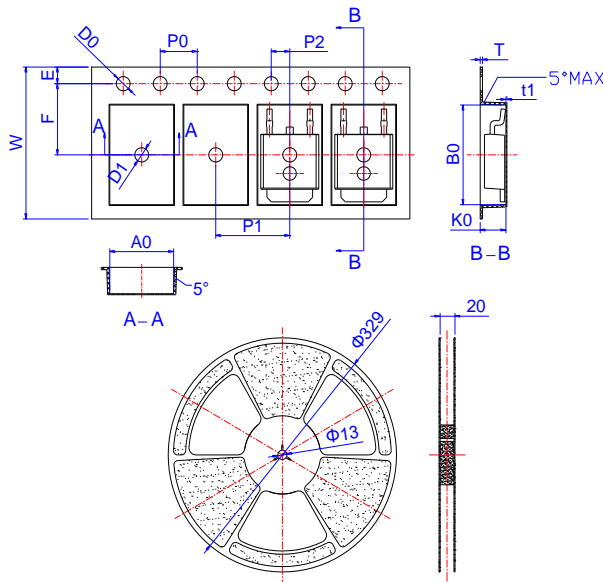
Package Mechanical Data



TO-252

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	2.10		2.50	0.083		0.098
A2	0		0.10	0		0.004
B	0.66		0.86	0.026		0.034
B2	5.18		5.48	0.202		0.216
C	0.40		0.60	0.016		0.024
C2	0.44		0.58	0.017		0.023
D	5.90		6.30	0.232		0.248
D1	5.30REF			0.209REF		
E	6.40		6.80	0.252		0.268
E1	4.63			0.182		
G	4.47		4.67	0.176		0.184
H	9.50		10.70	0.374		0.421
L	1.09		1.21	0.043		0.048
L2	1.35		1.65	0.053		0.065
V1		7°			7°	
V2	0°		6°	0°		6°

Reel Specification-TO-252



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
W	15.90	16.00	16.10	0.626	0.630	0.634
E	1.65	1.75	1.85	0.065	0.069	0.073
F	7.40	7.50	7.60	0.291	0.295	0.299
D0	1.40	1.50	1.60	0.055	0.059	0.063
D1	1.40	1.50	1.60	0.055	0.059	0.063
P0	3.90	4.00	4.10	0.154	0.157	0.161
P1	7.90	8.00	8.10	0.311	0.315	0.319
P2	1.90	2.00	2.10	0.075	0.079	0.083
A0	6.85	6.90	7.00	0.270	0.271	0.276
B0	10.45	10.50	10.60	0.411	0.413	0.417
K0	2.68	2.78	2.88	0.105	0.109	0.113
T	0.24		0.27	0.009		0.011
t1	0.10			0.004		
10P0	39.80	40.00	40.20	1.567	1.575	1.583